Listing and amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently amended) An apparatus for determining convergence of an equalizer, comprising:

an equalizer output signal;

a nearest element decision device, the nearest element decision device receiving the equalizer output signal and creating a decision device output signal containing permissible symbol values of a symbol constellation used in transmission of a signal to the apparatus; and

a monitoring circuit, the monitoring circuit receiving the decision device output signal and applying a test criterion to data contained in the decision device output signal so as to determine equalizer convergence.

2. (Previously presented) The apparatus of claim 1, wherein the equalizer is formed to include an infinite impulse response filter.

3. (Previously presented) The apparatus of claim 1, wherein the nearest element decision device is a slicer.

4. (Previously presented) The apparatus of claim 1, wherein the monitoring circuit receives the decision device output signal for a predetermined period of time representing an acquisition of a desired number of transmitted symbol values.

5. (Previously presented) The apparatus of claim 4, further comprising a memory, the memory being coupled to the monitoring circuit and being adapted to store decision device output data and test criteria.

6. (Previously presented) The apparatus of claim 5, wherein the test criteria for determining equalizer convergence includes identifying a desired sample of transmitted symbol values.

7. (Original) The apparatus of claim 6, wherein the desired sample of transmitted symbol values includes at least one of every possible symbol value.

8. (Previously presented) The apparatus of claim 1, wherein the monitoring circuit is coupled to the equalizer, the monitoring circuit resetting the equalizer when the equalizer diverges.

9. (Previously presented) The apparatus of claim 1, wherein the monitoring circuit is coupled to the equalizer, the monitoring circuit resetting the equalizer when the equalizer achieves an invalid state.

10. (Previously presented) The apparatus of claim 1, wherein the equalizer output signal includes an image representative datastream containing data packets.

11. (Previously presented) The apparatus of claim 1, wherein the monitoring circuit is a microprocessor.

12. (Currently amended) An equalizer status monitoring device for use in a digital communication system, the device including an adaptive channel equalizer, a slicer and a monitoring circuit, wherein the digital communications system receives a vestigial sideband modulated signal containing high definition video information represented by a multiple level symbol constellation, the data having a data frame format constituted by a succession of data frames, the adaptive channel equalizer generating a first output signal which is input to the slicer, the slicer generating a second output signal which is input to the monitoring circuit, the second output signal containing permissible symbol values of a symbol constellation used in transmission of a signal in the digital communication system; the monitoring circuit applying a test

criteria to the second output signal to determine convergence of the adaptive channel equalizer.

13. (Previously presented) The system of claim 12, wherein the monitoring circuit is coupled to the adaptive channel equalizer and resets the adaptive channel equalizer when the adaptive channel equalizer diverges.

14. (Previously presented) The system of claim 12, wherein the monitoring circuit is coupled to the adaptive channel equalizer and resets the adaptive channel equalizer when the adaptive channel equalizer assumes an invalid state.

15. (Original) The system of claim 12, wherein the test criteria for determining convergence requires identifying at least some transmitted symbol values.

16. (Previously presented) The system of claim 12, wherein the adaptive channel equalizer further comprises an infinite impulse response filter.

17. (Original) The system of claim 12, wherein the test criteria for determining convergence requires identifying at least one of each possible transmitted symbol value.

18. (Previously presented) The system of claim 12 wherein the monitoring circuit is a microprocessor.

Cancel claim 19.

Cancel claim 20.

Cancel claim 21.

Cancel claim 22.

Cancel claim 23.

24. (New) A method for use in determining equalizer convergence, the method comprising the steps of:

slicing an equalizer output signal to provide a sequence of symbols, each symbol taken from a constellation of possible transmitted symbols; and

testing at least a plurality of symbols of the sequence to determine if the equalizer is converged or not.

25. (New) The method of claim 24, wherein the constellation comprises an alphabet of N symbols, where $N > 1$, and the testing step determines that the equalizer is converged if at least M of the N symbols of the alphabet are represented in the plurality of symbols, where $M > 1$.

26. (New) The method of claim 24, wherein M equals N.